REMARKS

Claims 1-39 are active and pending in the present application; all of which stand rejected. Claims 14-39 stand rejected under 35 U.S.C. § 101 and claims 1-39 stand rejected under 35 U.S.C. § 103 as unpatentable over Van Hook (US Patent No. 6,266,758) in view of Motorola MC68030 users manual. In response, the following remarks are provided and new claims 40-84 are presented.

Support for Claims 40-84

New claims 40-84 are fully supported by the present specification. Support for specific claim elements is identified below by citing to the present specification as published (United States Pub. No. US 2004/0098567.

Regarding claim 40, the recited data processing system comprising in part "(a) a bus coupling components in the data processing system; (b) an external memory coupled to the bus; (c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising: an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path" is described at Figure 1 and paragraphs 0078 – 0081.

Regarding claim 40, the recited data processing system "wherein in response to decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a

destination register, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 41, the recited claim feature "wherein the execution unit is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0031, 0255 and 0261.

Regarding claim 42, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0255 and 0261.

Regarding claim 43, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Regarding claim 44, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction" is described at Figures 43A-C and paragraph 0255.

Regarding claim 45, the recited data processing system comprising in part "(a) a bus coupling components in the data processing system; (b) an external memory coupled to the bus; (c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising: an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the

stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path" is described at Figure 1 and paragraphs 0078 – 0081.

Regarding claim 45, the recited data processing system "wherein in response to decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with zeros to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 46, the recited claim feature "wherein the execution unit is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit unsigned integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081,0255 and 0261.

Regarding claim 47, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0255 and 0261.

Regarding claim 48, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Application No.: 10/712,430

Regarding claim 49, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0255.

Regarding claim 50, the recited data processing system comprising in part "(a) a bus coupling components in the data processing system; (b) an external memory coupled to the bus; (c) a programmable microprocessor coupled to the bus and capable of operation independent of another host processor, the microprocessor comprising: an instruction path; a data path; a plurality of registers operable to receive and store data from the data path and communicate the stored data to the data path; and an execution unit coupled to the instruction path and the data path and operable to decode and execute instructions received from the instruction path" is described at Figure 1 and paragraphs 0078 – 0081.

Regarding claim 50, the recited data processing system "wherein in response to decoding a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, the execution unit is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the most significant bit by the shift amount and fill a shift amount number of least significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 51, the recited claim feature "wherein the execution unit is operable to execute group shift left instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 52, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0255 and 0261.

Regarding claim 53, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Regarding claim 54, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0255.

Regarding claim 55, the recited group shift instruction in a computer-readable medium "specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift right instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 56, the recited claim feature "wherein the computer system is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 57, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0255 and 0261.

Regarding claim 58, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Regarding claim 59, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0255.

Regarding claim 60, the recited group shift instruction in a computer-readable medium "specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift right instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with zeros to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 61, the recited claim feature "wherein the computer system is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit unsigned integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 62, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 63, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Regarding claim 64, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0255.

Regarding claim 65, the recited group shift instruction in a computer-readable medium "specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift left instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the most significant bit by the shift amount and fill a shift amount number of least significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 66, the recited claim feature "wherein the computer system is operable to execute group shift left instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Application No.: 10/712,430

Regarding claim 67, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 68, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Regarding claim 69, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0255.

Regarding claim 70, the recited "computer data signal embodied in a transmission medium: having instructions that cause a computer system to perform operations, the instructions including a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift right instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 71, the recited claim feature "wherein the computer system is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 72, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 43A-C and 43H-J, and paragraphs 0255 and 0261.

Regarding claim 73, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Regarding claim 74, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0255.

Regarding claim 75, the recited "computer data signal embodied in a transmission medium: having instructions that cause a computer system to perform operations, the instructions including a single group shift right instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift right instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the least significant bit by the shift amount and fill a shift amount number of most significant bits with zeros to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 76, the recited claim feature "wherein the computer system is operable to execute group shift right instructions on 16-bit, 32-bit and 64-bit unsigned integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 77, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 78, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Regarding claim 79, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0255.

Regarding claim 80, the recited "computer data signal embodied in a transmission medium: having instructions that cause a computer system to perform operations, the instructions including a single group shift left instruction specifying a shift amount, an operand register containing a plurality of equal-sized data elements stored in partitioned fields of the operand register and a destination register, wherein in response to the single group shift left instruction, the computer system is operable to: (i) for each of the plurality of data elements in the operand register, shift a subfield of the data element towards the most significant bit by the shift amount and fill a shift amount number of least significant bits with the sign bit of the respective data element to produce a second plurality of equal-sized data elements and (ii) provide the second plurality of data elements as a catenated result to the destination register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 81, the recited claim feature "wherein the computer system is operable to execute group shift left instructions on 16-bit, 32-bit and 64-bit signed integer data" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 82, the recited claim feature "wherein the operand register is a 128-bit register and the destination register is a 128-bit register" is described at Figures 1, 43A-C and 43H-J, and paragraphs 0081, 0255 and 0261.

Regarding claim 83, the recited claim feature "wherein the shift amount is contained in an immediate field of the instruction" is described at Figures 43H-J, and paragraph 0261.

Regarding claim 84, the recited claim feature "wherein the shift amount is contained in a register specified by the instruction." is described at Figures 43A-C and paragraph 0255.

Rejection under 35 U.S.C. § 101

The Examiner has rejected Claims 14–39 as directed to non-statutory subject matter under 35 U.S.C. § 101. According to the Examiner, the claims are directed to a "medium" or "signal" that is not tangible and therefore not statutory subject matter. Applicants respectfully disagree. The Examiner bears the *prima facie* burden of establishing that the claims are not directed to patentable subject matter. See MANUAL OF PATENT EXAMINING PROCEDURES ("MPEP") § 2106.

The breadth of subject matter appropriate for patenting is extraordinarily broad: statutory subject matter encompasses "anything under the sun that is made by man." See id. (quoting *Diamond v. Chakrabarty*, 447 U.S. 303, 308-09 (1980)) (emphasis added). For this reason, the Federal Circuit has strongly cautioned against reading unwritten limitations into section 101:

> The repetitive use of the expansive term "any" in § 101 shows Congress's intent not to place any restrictions on the subject matter for which a patent may be obtained beyond those specifically recited in § 101. Indeed, the Supreme Court has acknowledged that Congress intended § 101 to extend to "anything under the sun that is made by man." Thus, it is improper to read limitations into § 101 on

> the subject matter that may be patented where the legislative history indicates that Congress clearly did not intend such limitations.

See *State Street Bank & Trust Co. v. Signature Financial Group, Inc.*, 149 F.3d 1368, 1373 (Fed. Cir. 1998) (internal citation and footnote omitted) (emphasis added). Here, the Examiner has imported into section 101 a requirement that conflicts with the guiding principle that "anything under the sun that is made by man" is patentable subject matter. It is beyond dispute that the "computer-readable medium"[1] and "computer data signal, embodied in a transmission medium"[2] recited in Claims 14–39 are "made by man."

Consistent with the extensive scope of section 101, the MPEP recognizes that the only types of subject matter not eligible for patenting are abstract ideas, laws of nature and natural phenomena:

> The subject matter courts have found to be outside the four statutory categories of invention is limited to abstract ideas, laws of nature and natural phenomena. . . . These three exclusions recognize that subject matter that is not a practical

---

[1] For example, independent Claim 14 from which Claims 15–26 each depend recites:

> 14. A computer-readable medium: having instructions that cause a computer system to perform operations, wherein at least some of the instructions comprise a group shift instruction for shifting data in a programmable processor, the group shift instruction: specifying both a shift amount and a register having a register width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the shift amount configurable to an amount inclusively between zero and one less than the elemental width; shifting a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data elements; and providing the second plurality of data elements as a catenated result.

[2] For example, independent Claim 27 from which Claims 28–39 each depend recites:

> 27. A computer data signal, embodied in a transmission medium: having instructions that cause a computer system to perform operations, wherein at least some of the instructions comprise a group shift instruction for shifting data in a programmable processor, the group shift instruction: specifying both a shift amount and a register having a register width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the number of data elements in the first plurality of data elements being inversely related to the elemental width, the shift amount configurable to an amount inclusively between zero and one less than the elemental width; shifting a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data elements; and providing the second plurality of data elements as a catenated result.

> application or use of an idea, a law of nature or a natural phenomenon is not patentable.

MPEP 2106 (emphasis in original). The Examiner has not sought to—and presumably recognizes that it would be improper to—characterize the subject matter of the rejected claims as abstract ideas, laws of nature and natural phenomena. Nor could the Examiner reasonably assert that the claimed "computer-readable medium" and "computer data signal, embodied in a transmission medium" do not have a practical use or application.

Although the patentability of software was at one time undecided, the courts and the PTO have resolved this issue. Indeed, the MPEP specifically recognizes the propriety of claiming a "computer-readable medium" (indeed, in those words) that contains "functional descriptive material" such as software:

> When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized.

See MPEP § 2106 (emphasis added). This same rationale is pertinent here: in Claims 14–26, the software instructions are embodied in the "computer-readable medium" and the nature of the "computer-readable medium" enables the function of the software materials to be realized.

Although Applicants located no court case that directly addresses the subject matter issue for claims to a "computer-readable medium," the Federal Circuit's recent decision in *Schumer v. Laboratory Computer Sys., Inc.*, 308 F.3d 1304 (Fed. Cir. 2002) is instructive. Like the "computer-readable medium" recited in rejected Claims 14–26, one of the claims in *Schumer* recited "[a] computer readable medium containing a computer program which program causes a computer to perform the method of claim 13." See id. at 1308 (emphasis added). Importantly, neither the parties nor the court in *Schumer* even suggested that the claim was improper subject

matter. See id. To the contrary, the issues in that case related to whether the claims were infringed or rendered invalid by the prior art. See id. at 1310–17. Thus, the parties and the court implicitly assumed that the claim to a "computer readable medium" was proper subject matter under section 101.

The Examiner's rejection of Claims 27–39 under section 101 is similarly misplaced. Like the "computer-readable medium" claims, the claims reciting a "computer data signal, embodied in a transmission medium" satisfy the general "made by man" rule and do not fall into one of the three excluded categories (*i.e.*, abstract ideas, laws of nature and natural phenomena). Moreover, these claims also involve "functional descriptive material" that is recorded on a "computer-readable medium" and therefore further satisfy the rationale of MPEP § 2106. In addition, the MPEP also explicitly provides that "a signal claim directed to a practical application of electromagnetic energy is statutory regardless of its transitory nature." See MPEP 2106. Thus, the patentability of these claims does not turn on the specific nature of the transmission medium.

Claims 14–39 recite subject matter that is "made by man" and is not excluded from patentability as abstract ideas, laws of nature or natural phenomena. Furthermore, the claimed subject matter falls within categories recognized as patentable by the Federal Circuit and MPEP. Because the claimed subject matter is statutory under section 101, Applicants respectfully request that the Examiner withdraw the section 101 subject matter rejections.

Rejection under 35 U.S.C. § 103

Regarding the obviousness rejections, the primary Van Hook reference does not qualify as prior art to the pending claims, because the present application claims priority back to the

August 16, 1995, filing date of U.S. Patent No. 5,742,840 (the '840 patent), as indicated by the priority claim, which is hereby reproduced for the convenience of the Examiner:

> "This application is a continuation of U.S. Patent Application No. 09/922,319, filed August 2, 2001, [now U.S. Patent No. 6,725,356 issued on April 20, 2004,] which is a Continuation of U.S. Patent Application No. 09/382,402, filed August 24, 1999, now U.S. Patent No. 6,295,599, which claims the benefit of priority to Provisional Patent Application No. 60/097,635 filed August 24, 1998, and is a continuation-in-part of U.S. Patent Application No. 09/169,963, filed October 13, 1998, now U.S. Patent No. 6,006,318, which is a continuation of U.S. Patent Application No. 08/754,827, filed November 22, 1996 now U.S. Patent No. 5,822,603, which is a divisional of U.S. Patent Application No. 08/516,036, filed August 16, 1995 now U.S. Patent No. 5,742,840."

Support for all the pending claims is found in the disclosure of the '840 patent. Van Hook's filing date was March 5, 1999, more than one year later than the August 15, 1995 filing date of the '840 patent. Therefore, Van Hook is not prior art to the claims of the present application.

As the priority claim states, U.S. Patent 6,295,599 ("the '599 patent" is in the direct chain of priority for the present application. Applicants note that various amendments were made to the specification of the '599 patent for submission as the specification of the present application. However, no new matter was added, since the amendments to the specification were made exclusively by inserting materials from the appendix of the '599 patent ("the '599 appendix"). The '599 appendix is (a) attached as an appendix in microfiche form in the '599 patent, (b) attached in CD-ROM format and incorporated by reference in U.S. Patent Application No. 09/922,319, which is a continuation of the '599 patent and the immediate parent of the present application.

To provide support for the claims and comply with MPEP 608.01(i), amendments were made to the specification of the '599 patent for submission in the present specification, which included adding both text and new Figs. 12 through 49G from the '599 appendix, primarily

related to different embodiments of various instructions that the invention is capable of executing. Many of these specific instructions are illustratec in new Figs. 31A through 47C, which are reproduced directly from the '599 appendix. Text corresponding to Figs. 31A through 47C is derived from the '599 appendix and describes the specific processor instructions set forth in those figures.

Pending claims 1-39 are fully supported by the '840 patent and its appendix ("the '840 appendix"), as well as by the '599 patent and the '599 appendix. Thus, claims 1-39 should be accorded an effectively filing date of August 16, 1995. Support for specific claim elements in both the '840 patent and the '599 patent is provided below.

The recited data processing system includes a bus (70) described in Fig. 5 of the '840 patent with, as also shown in FIG. 5, an external memory (74) (See also, FIG. 6, elements 88 and 90). A programmable processor, as recited in claim 1, is described in the '840 patent at col. 4, lines 2-5 and in the '599 patent at col. 1, lines 56-60 and col. 15 line 9. A virtual memory addressing unit is described in the '840 patent at col. 15, line 66 through col. 16, line 8 and in the '599 patent at col. 15, line 9. A data path is described in the '840 patent at col. 4, lines 27-28 and in the '599 patent at col. 5, lines 8-10; and an instruction path is described, for example, in the '840 patent at col. 14, lines 11-26. A register file, as recited, is described in the '840 patent at col. 4, lines 33-35 and in the '599 patent at col. 4, lines 18-19. As shown in Fig. 1 of the '599 patent, a cache memory 117 is arranged in communication with a bus interface 118, as recited in claim 1 as well. An execution unit is described in the '840 patent at col. 4, lines 35-38 and in the '599 patent at col. 5, lines 44 and 51-56 with the capability to execute and decode instructions. .

In particular, claim 1 also recites that decoding a single instruction specifying both a shift amount and a register having a register width, the number of data elements in the first plurality of

data elements being inversely related to the elemental width, the register containing a first plurality of data elements having an elemental width smaller than the register width, the shift amount configurable to an amount inclusively between zero and one less than the elemental width, the execution unit is operable to: (i) shift a subfield of each of the first plurality of data elements by the shift amount to produce a second plurality of data elements; and (ii) provide the second plurality of data elements as a catenated result. In the present application, this functionality is described in more detail starting at paragraph [0229]. Exemplary instructions that include this specific functionality are described in the '599 Appendix and the '840 Appendix, for example, and include

(a) G.SHR, G.U.SHR G.SHR.I, G.U.SHR.I (described in the '840 appendix at pages 103-105, 119)

(b) X.SHR, X.SHR.U, X.SHR.I, X.SHR.I.U (described in the '599 appendix at pages 188, 206)

(c) G.EXTRACT.I, G.COMPRESS (described in the '840 appendix at pages 110, 126)

(d) X.EXTRACT, X.COMPRESS, Ensemble EXTRACT (described in the '599 appendix at pages 192).

With regard to claim 2, the '840 Appendix, at page 106, explains the result is placed in a register specified by "rc". With regard to claim 3, the description of the instruction at page 106 explains the use of values in the registers and, with regard to claim 4, at page 112, the operation of the instruction having the specified shift amount is described. With regard to claims 5 – 7, the pseudo code, for example, on pages 106-109 with respect to G.SHR and G.U.SHR detail how the specific bits of the instructions and registers are defined and aligned.

With respect to claims 8-10, the table on page 106 (of the '840 Appendix) illustrates instructions utilizing 16, 32, and 128 bits. With respect to claims 11-13, the programmable nature of the claimed processor and the flexibility with which the elemental widths of the

different data elements may be specified within an instruction support the specific relative data sizes recited in these claims.

Claims 14-26 recite claim features similar to those recited in claims 1-13 wherein claims 1-13 relate to a data processing system and claims 14-26 relate to a computer readable medium having instructions that cause such a system to perform appropriately. Claims 27-39 relate to a computer data signal that is embodied in a transmission media, wherein the instructions cause a similar system to perform operations analogous to those recited in claims 1-13 and 14-26. Accordingly, the support in the '599 Appendix and the '840 Appendix identified with regard to claims 1-13 is also applicable to claims 14-26 and claims 27-39.

As illustrated, all pending claims are supported by the '840 patent and/or the '840 appendix, and the '599 patent and/or the '599 appendix. That is, all pending claims 1-39 have a priority date back to August 1995, which predates Van Hook. Thus, Van Hook does not qualify as a prior art reference for purposes of the Examiner's obviousness rejection. Therefore, Applicants respectfully request that rejections of claims 1-39 under 35 U.S.C. § 103(a) be withdrawn. Furthermore, the newly added claims 40-84 are also supported by the earlier disclosures and are entitled to a priority date which predates Van Hook.

Accordingly, it is believed that all pending claims are now in condition for allowance. Applicants therefore respectfully request an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicants' representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

Application No.: 10/712,430

including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Wesley L. Strickland

Wesley L. Strickland
Registration No. 44,363

4370 La Jolla Village Drive, Suite 700
San Diego, CA 92122
Phone: 858.535.9001 WLS:bsl
Facsimile: 858.597.1585
Date: September 11, 2006

Please recognize our Customer No. 41552 as our correspondence address.

SDO 49695-1.043876.0148